

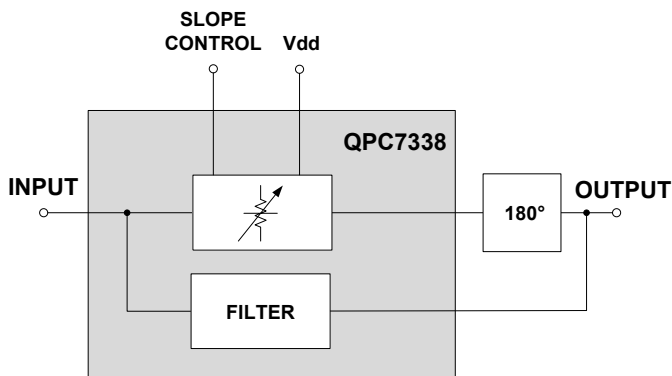
### Product Description

The QPC7338 is a cable compensated voltage controlled variable equalizer employing SOI attenuator with operation bandwidth from 108MHz to 1794MHz, optimized for operation between 258MHz and 1794MHz.



14 pin, 6.0 mm x 6.0 mm x 1.375 mm package

### Functional Block Diagram



### Product Features

- 108 – 1794 MHz Operational Bandwidth
- Inverse cable loss frequency response
- 18dB slope range
- Low insertion loss
- High linearity
- 75Ohm impedance for CATV applications
- 5V single-supply voltage
- Low power consumption

### Applications

CATV amplifier and transmission systems

### Ordering Information

Part No.	Description
QPC7338SB	Sample bag 5 pcs
QPC7338SR	7" Reel with 100 pcs
QPC7338TR7	7" Reel with 500 pcs
QPC7338PCBA-410	Fully assembled Evaluation Board

### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Supply Voltage (Vdd)		+5		V
Junction Temperature			+125	°C
Operating Mounting Base Temperature	-40		+100	°C

Electrical specifications are measured at specified test conditions in the application circuit. Specifications are not guaranteed over all recommended operating conditions.

### Absolute Maximum Ratings

Parameter	Value / Range
Supply Voltage (Vdd)	-0.5 to +6V
Control Voltage (Vc)	-0.5 to +6V
Control Voltage 2 (Vc2)	-2 to +24V
MODE	-0.5 to +6V
Storage Temperature	-40 to 100 °C
RF Input Power	+30 dBm

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Electrical Specifications – Tested in Evaluation Circuit

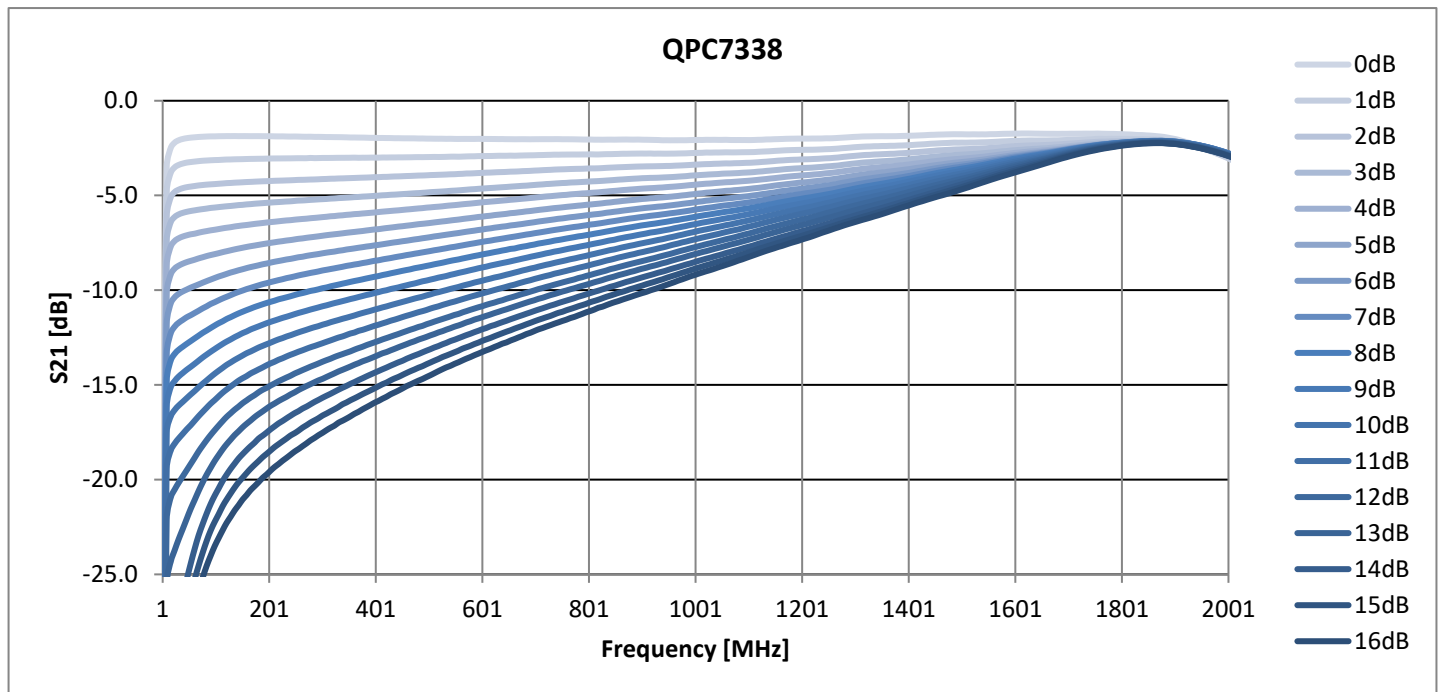
Parameter	Conditions (V <sub>dd</sub> =5V, T <sub>MB</sub> =25°C, Z <sub>S</sub> =Z <sub>L</sub> =75Ω)	Min	Typ	Max	Units
<b>General Performance</b>					
Supply Current (I <sub>dd</sub> )			3		mA
Thermal Resistance			70		K/W
RF Input Power	T ≤ +85°C			27	dBm
	+85°C < T ≤ +100°C			24	
Input IP3	P <sub>IN</sub> + (IM <sub>3dBc</sub> /2) 6MHz tone spacing at 15dBm/tone		50		dBm
Input IP2	P <sub>IN</sub> + IM <sub>2dBc</sub> , IM2 is F1 + F2 6MHz tone spacing at 15dBm/tone		80		dBm
<b>Frequency Range 108 to 1794MHz</b>					
Minimum Slope <sup>[1]</sup>	108 to 1794MHz		0.5		dB
Maximum Slope <sup>[1]</sup>	108 to 1794MHz		18		dB
<b>RF Performance, slope set between 4dB (2.4dB/GHz) and 14dB (8.3dB/GHz)</b>					
Insertion Loss (S <sub>21</sub> )	1794MHz		2.2	2.5	dB
Flatness <sup>[2]</sup>	108 to 1794MHz		0.5	0.6	dB
Input Return Loss (-S <sub>11</sub> )	108 to 1794MHz		17		dB
Output Return Loss (-S <sub>22</sub> )	108 to 1794MHz		17		dB
<b>RF Performance, slope set between 0.5dB (0.3dB/GHz) and 18dB (10.7dB/GHz)</b>					
Insertion Loss (S <sub>21</sub> )	1794MHz		2.3		dB
Flatness <sup>[2]</sup>	108 to 1794MHz		1.3		dB
Input Return Loss (-S <sub>11</sub> )	108 to 1794MHz		16		dB
Output Return Loss (-S <sub>22</sub> )	108 to 1794MHz		16		dB
<b>Frequency Range 258 to 1794MHz</b>					
Minimum Slope <sup>[1]</sup>	258 to 1794MHz		0.1		dB
Maximum Slope <sup>[1]</sup>	258 to 1794MHz		16		dB
<b>RF Performance, slope set between 4dB (2.6dB/GHz) and 14dB (9.1dB/GHz)</b>					
Insertion Loss (S <sub>21</sub> )	1794MHz		2.3	2.5	dB
Flatness <sup>[2]</sup>	258 to 1794MHz		0.5	0.6	dB
Input Return Loss (-S <sub>11</sub> )	258 to 1794MHz		17		dB
Output Return Loss (-S <sub>22</sub> )	258 to 1794MHz		17		dB
<b>RF Performance, slope set between 0.1dB (0.06dB/GHz) and 16dB (10.4dB/GHz)</b>					
Insertion Loss (S <sub>21</sub> )	1794MHz		2.4		dB
Flatness <sup>[2]</sup>	258 to 1794MHz		0.6		dB
Input Return Loss (-S <sub>11</sub> )	258 to 1794MHz		16		dB
Output Return Loss (-S <sub>22</sub> )	258 to 1794MHz		16		dB

Parameter	Conditions (V <sub>dd</sub> =5V, T <sub>MB</sub> =25°C, Z <sub>S</sub> =Z <sub>L</sub> =75Ω)	Min	Typ	Max	Units
<b>Control</b>					
Control Voltage (Vc) <sup>[3]</sup> , positive slope control gradient	MODE = 0V, minimum slope at Vc = 0V	0	1 to 3	5	V
Control Voltage (Vc) <sup>[3]</sup> , negative slope control gradient	MODE = 5V, minimum slope at Vc = 5V	0	2 to 4	5	V
Control Voltage 2 (Vc2) <sup>[3]</sup> , positive slope control gradient	MODE = 0V, minimum slope at Vc2 = 0V	0	4 to 12	20	V
Control Voltage 2 (Vc2) <sup>[3]</sup> , negative slope control gradient	MODE = 5V, minimum slope at Vc2 = 20V	0	8 to 16	20	V
MODE Pin Logic Low				0.4	V
MODE Pin Logic High		1			V

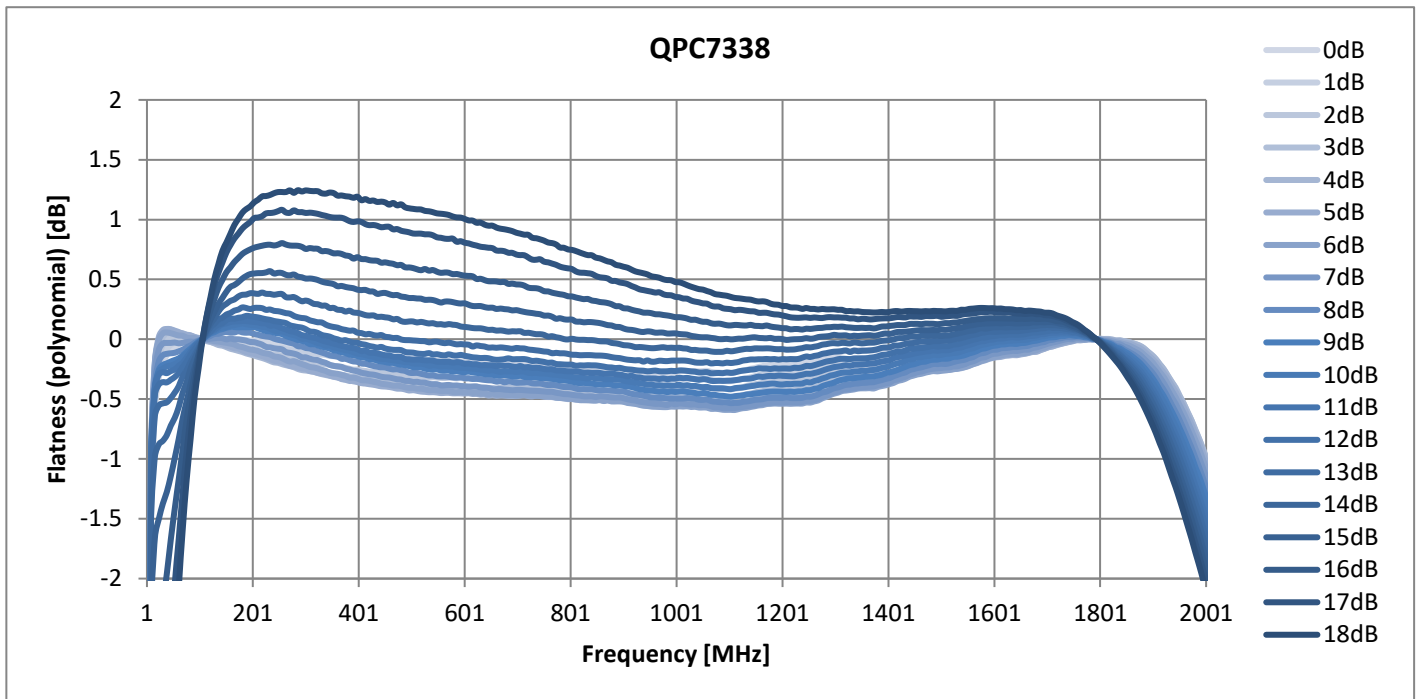
Notes:

1. Slope is defined as the difference between the gain at the start frequency and the gain at the stop frequency.
2. Flatness is defined as sum of positive and negative deviation from a polynomial inverse to the typical cable loss between gain at start frequency and gain at stop frequency. The cable loss/100ft is here defined by the polynomial  $-(0.175 \cdot \sqrt{f[\text{MHz}]}) + 0.001 \cdot f[\text{MHz}]$ .
3. Either Vc or Vc2 can be used to set slope, internal 1:4 voltage divider between Vc and Vc2.

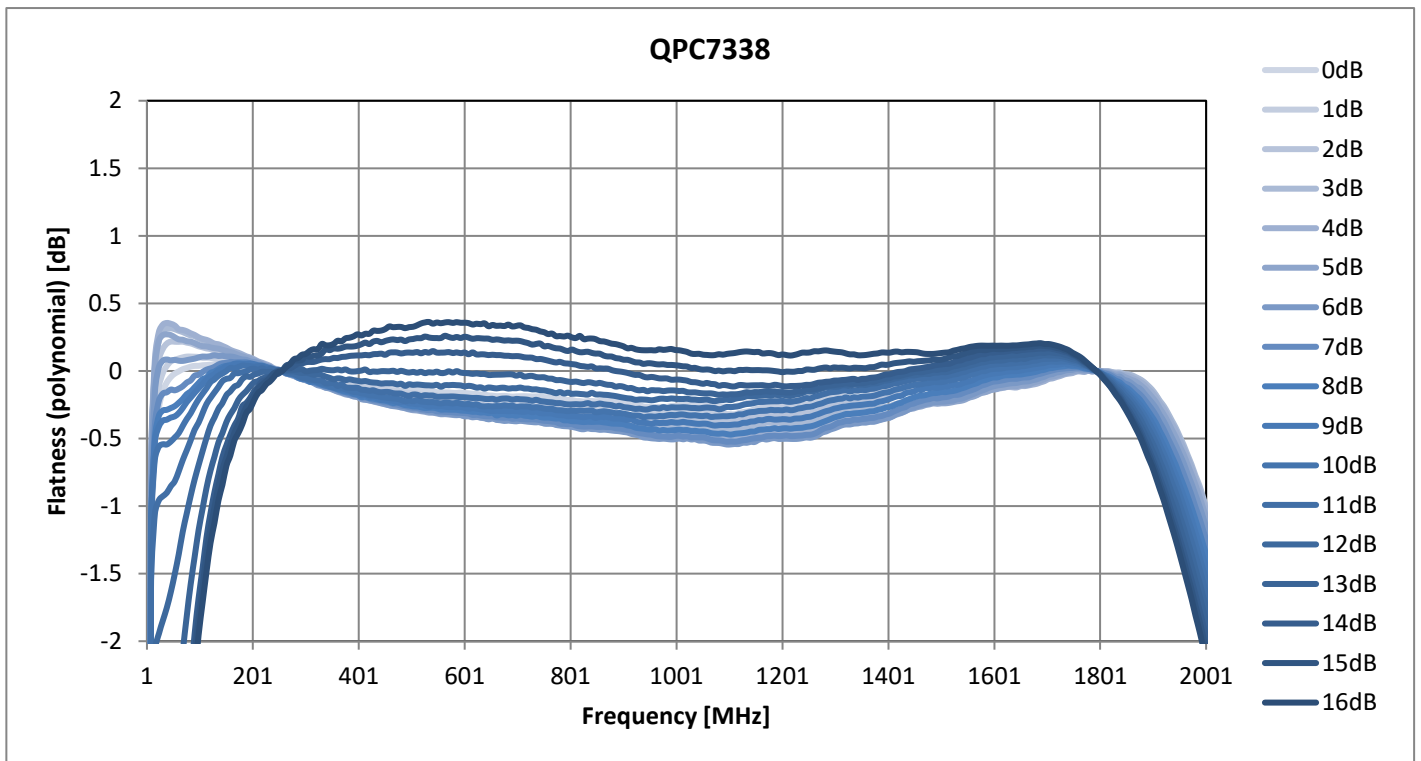
QPC7338 Slope vs. Frequency, typical (258 to 1794MHz)



QPC7338 Flatness vs. Slope, typical (108 to 1794 MHz)

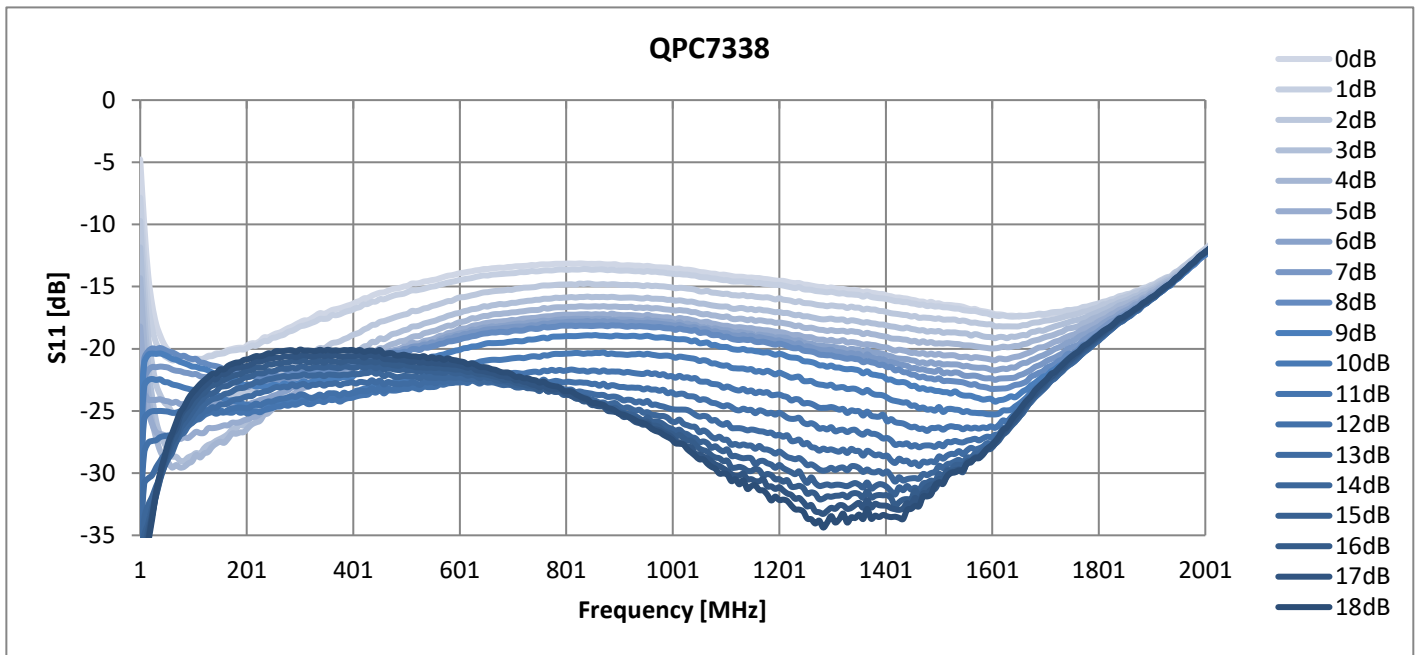


QPC7338 Flatness vs. Slope, typical (258 to 1794 MHz)

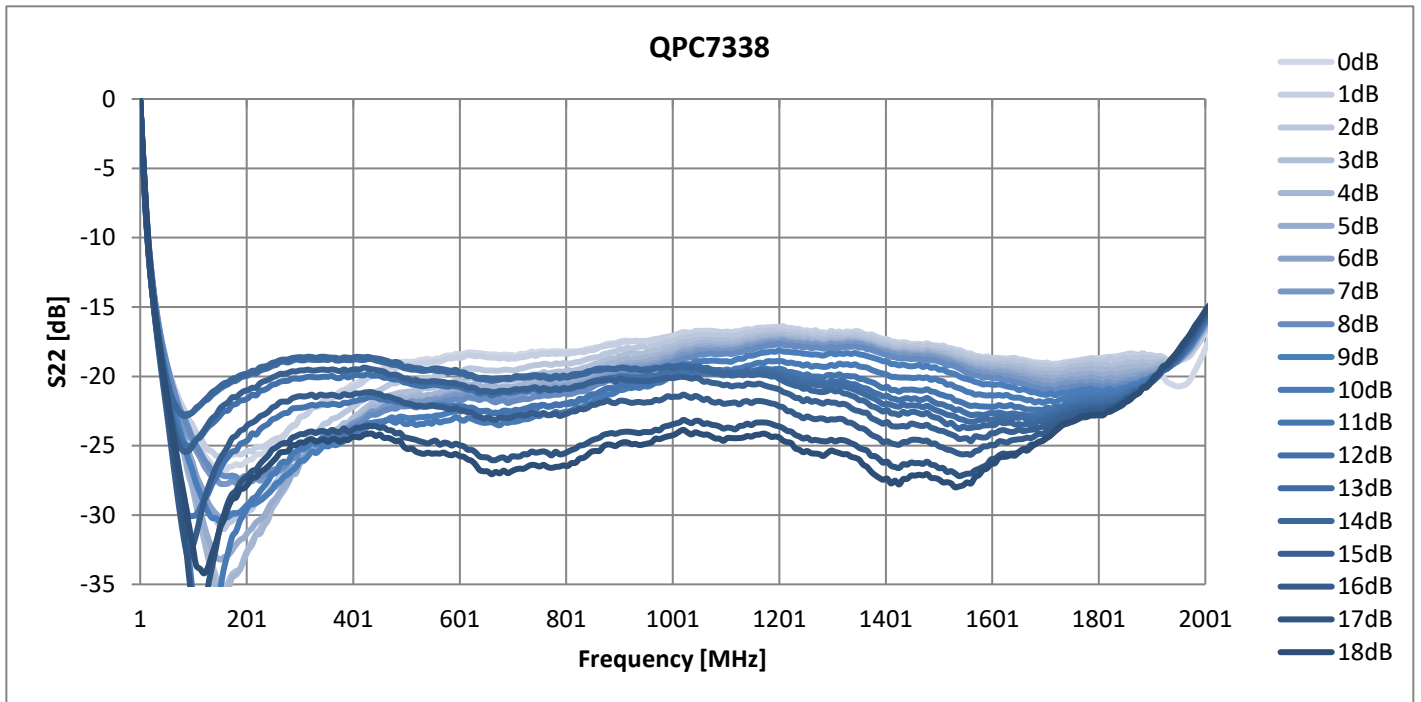


Flatness is measured against a polynomial inverse to the typical cable loss/100ft of  $-(0.175 \cdot \sqrt{f[\text{MHz}]} + 0.001 \cdot f[\text{MHz}])$

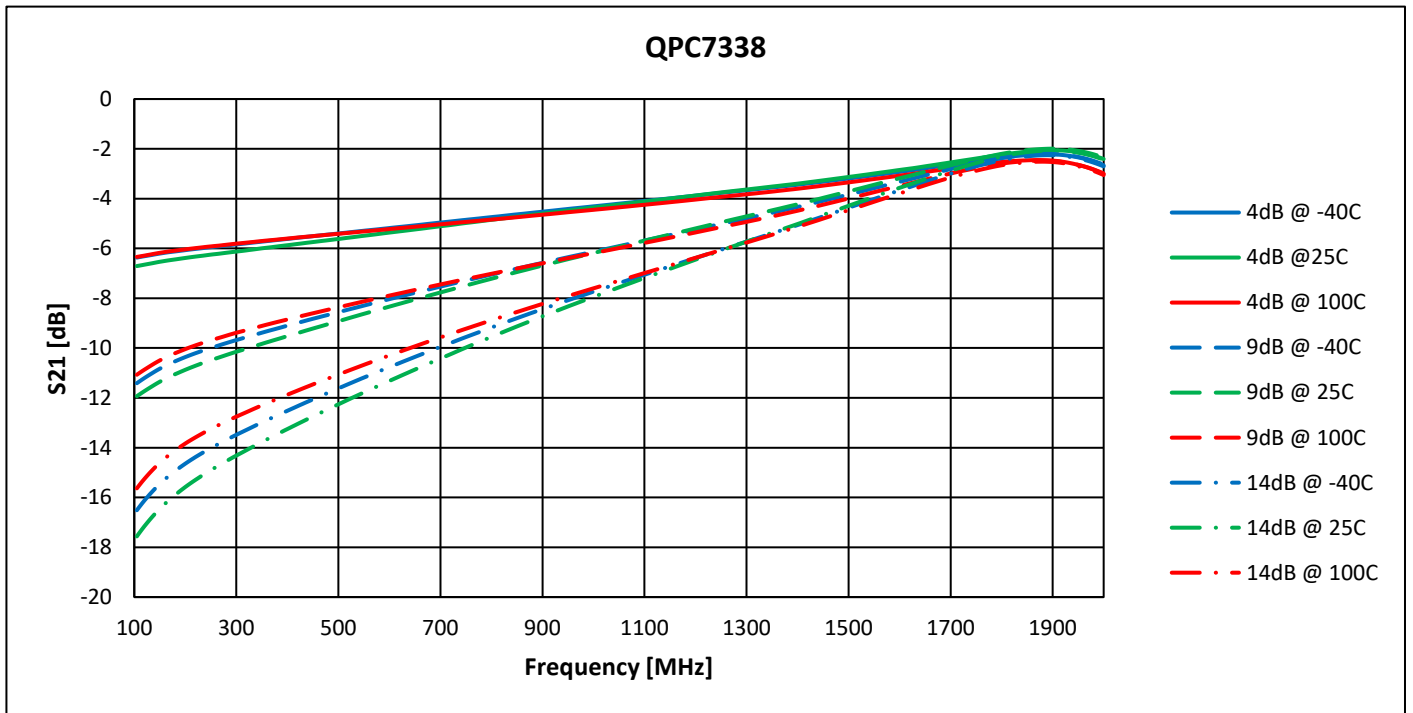
QPC7338 S11 vs. Slope, typical (108 to 1794MHz)



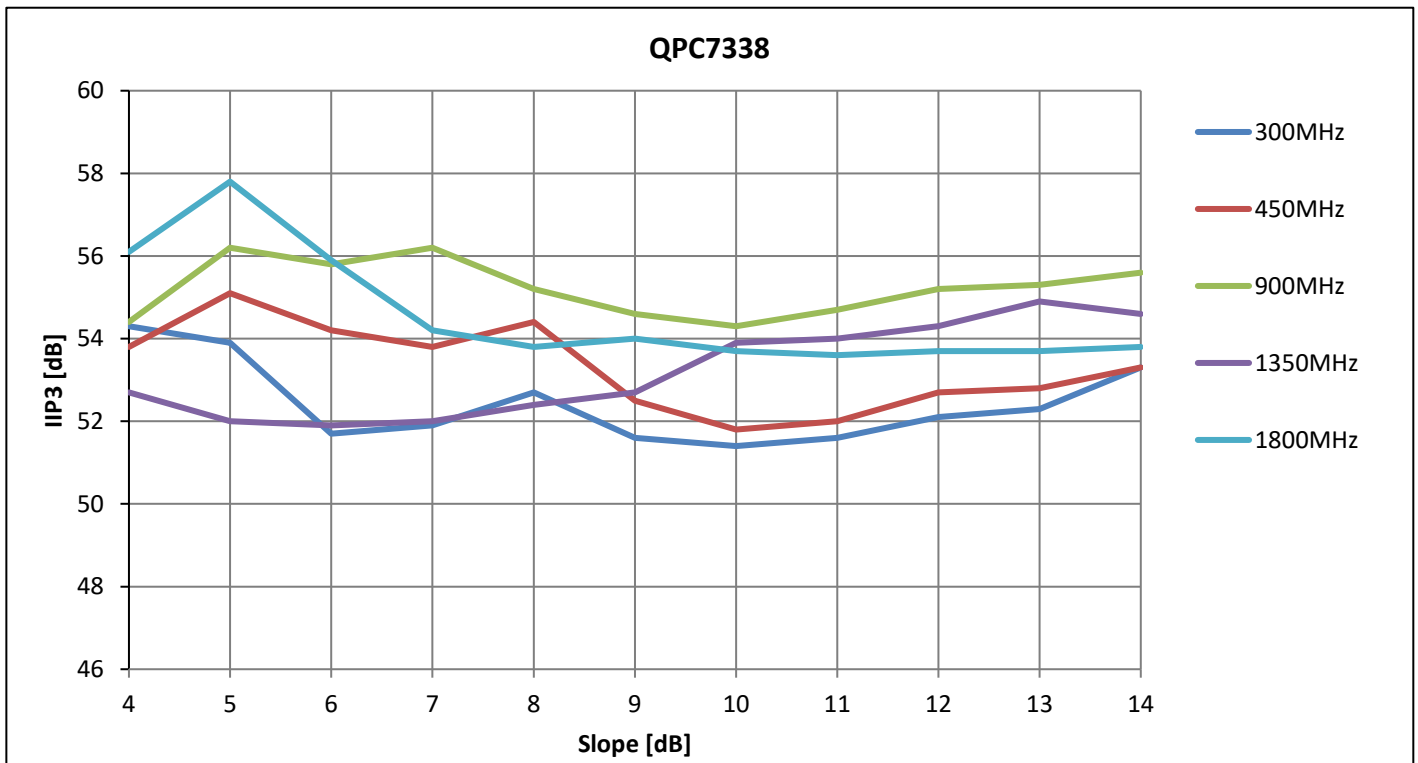
QPC7338 S22 vs. Slope, typical (108 to 1794MHz)



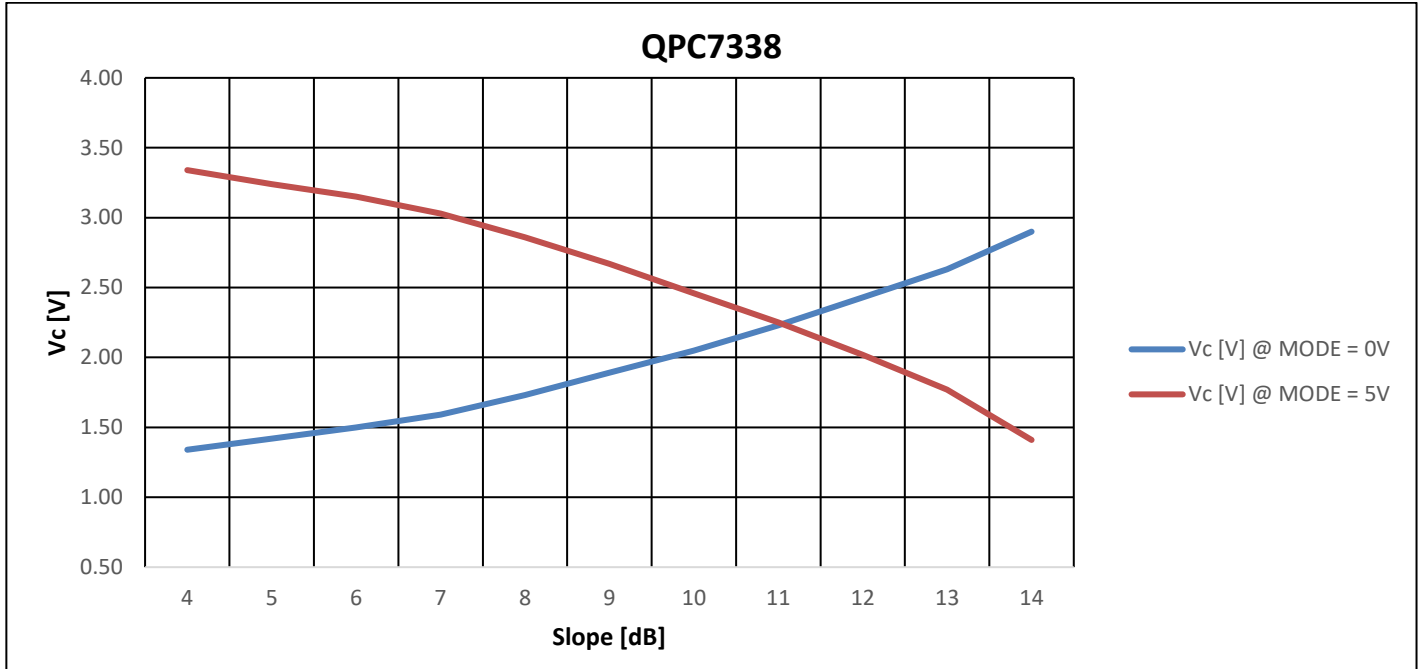
QPC7338 Slope vs. Temperature, typical (108 to 1794MHz)



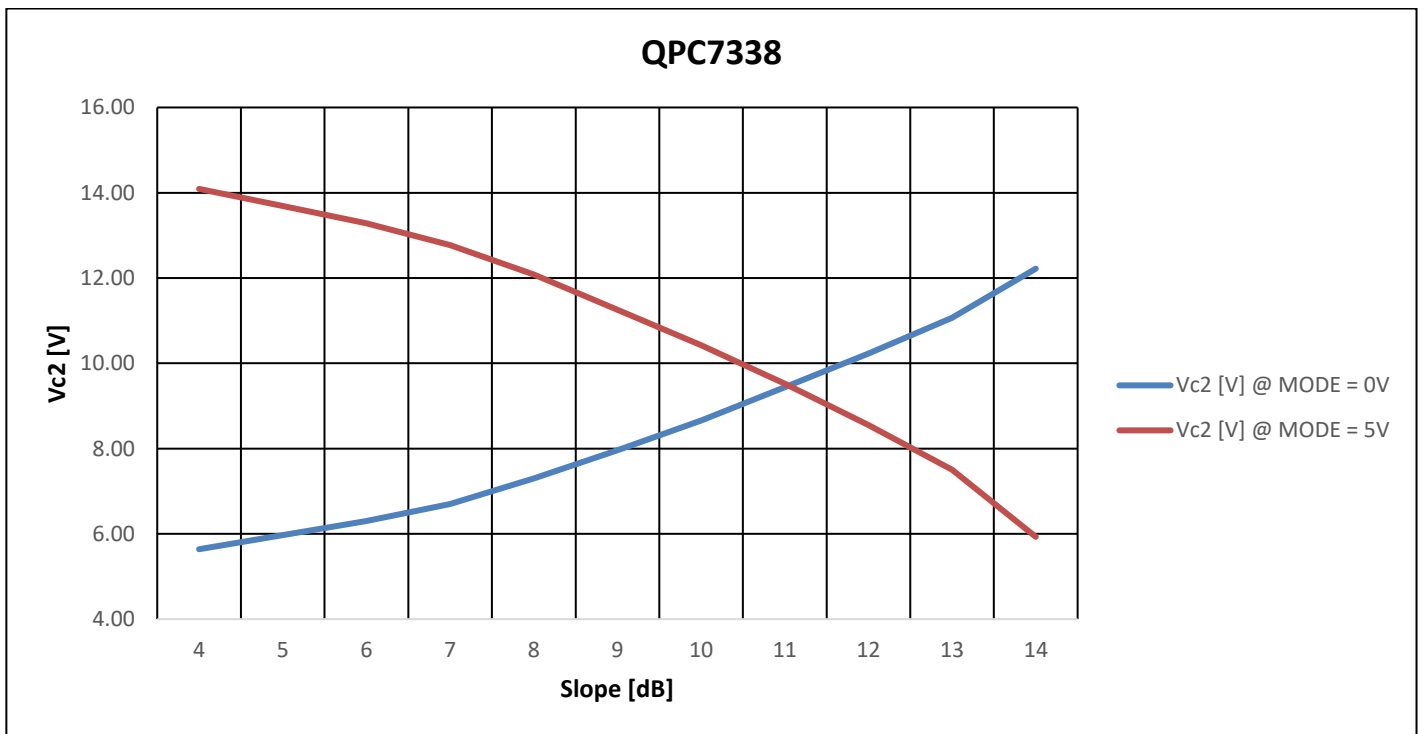
QPC7338 Input IP3 (258 to 1794MHz) @ 25°C



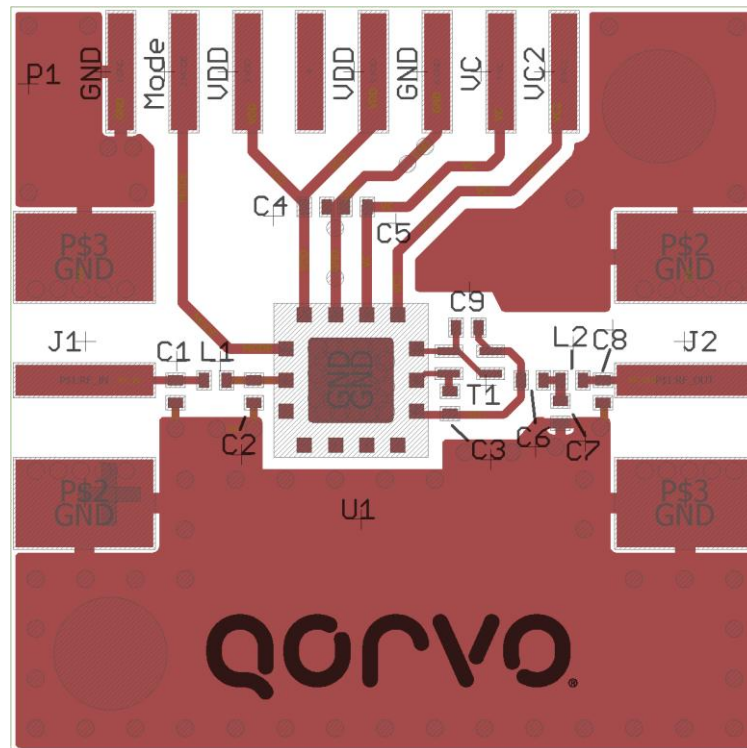
QPC7338 Slope vs. Vc, typical



QPC7338 Slope vs. Vc2, typical

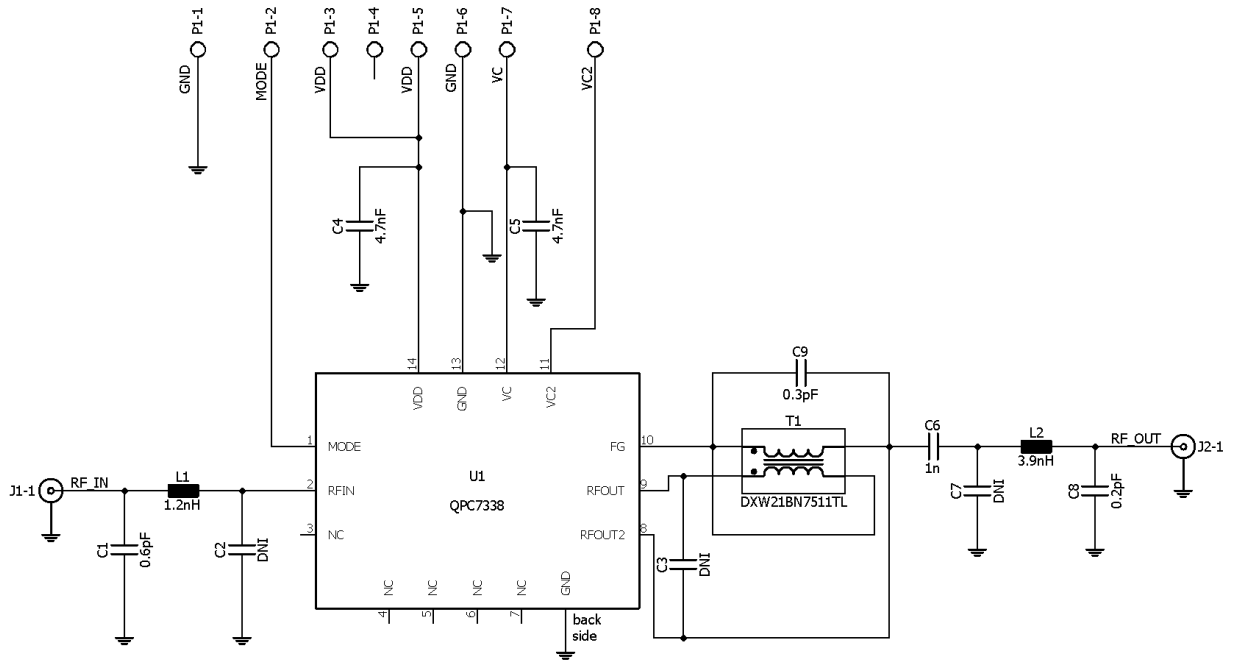


Evaluation Board Assembly Drawing



The ground plane of the QPC7338 module should be soldered onto a board equipped with thermal vias. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25mm (0.010").  
 Evaluation board PCB: FR4, double sided, 1.5mm, 35um Cu

## Evaluation Board Schematic

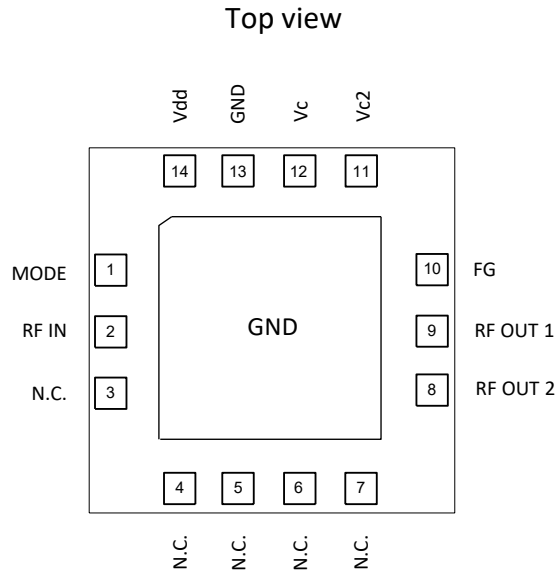


## Evaluation Board Bill of Materials (BOM)

Ref. Designator	Value, package	Description	Manufacturer	Part Number
C1	0.6pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C2, C3, C7	DNI			
C4, C5	4.7nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C6	1nF, X7R, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C9	0.3pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
C8	0.2pF, C0G, 0402	Chip capacitor	MURATA, TAIYO YUDEN	
L1	1.2nH, 0402	Chip inductor	MURATA	LQG15
L2	3.9nH, 0402	Chip inductor	MURATA	LQG15
T1		Transformer	MURATA	DXW21BN7511TL08
J1, J2		Connector F-type, female	Amphenol	222181
P1		Connector, 2.54mm pin spacing, optional	various	
U1		Variable equalizer	QORVO	QPC7338

Notes: C1, L1, C9, L2 and C8 may be modified in target application circuit for S11 and S22 optimization

Pin Configuration

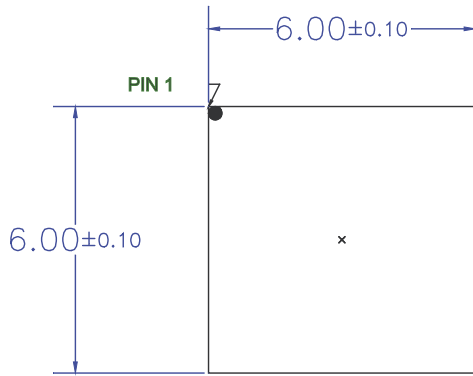


Pin Description

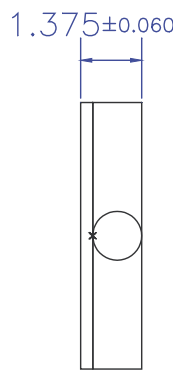
Pin No.	Label	Description
1	MODE	Slope control gradient (0V: positive slope control gradient or 5V: negative slope control gradient)
2	RF IN	RF input signal, AC coupled
8	RF OUT 2	Connection to balun and circuit output
9	RF OUT 1	Connection to balun
10	FG	Floating ground, connection to balun
11	Vc2	Control voltage 2
12	Vc	Control voltage
13, GND	GND	Ground
14	Vdd	+5V supply voltage
3, 4, 5, 6, 7	N.C.	Not connected

Notes: Either Pin11 or Pin12 can be used to set slope, internal 1:4 voltage divider between Pin11 and Pin12

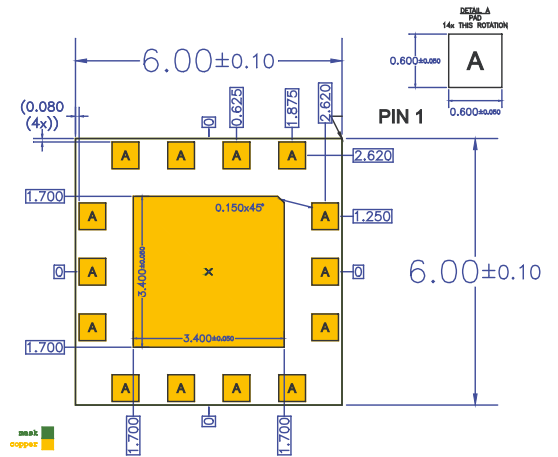
Package Outline Drawing (Dimensions in millimeters)



TOP VIEW



SIDE VIEW

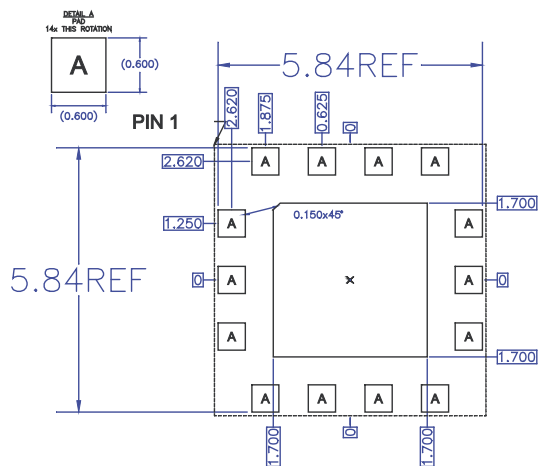


BOTTOM VIEW

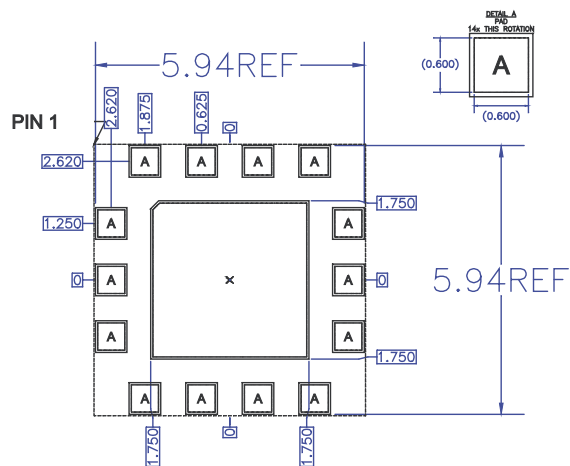
Notes:

1. Dimension and tolerance formats conform to ASME Y14.5M-1994.
2. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.
3. Co-planarity applies to the exposed ground/thermal pad as well as the contact pins.
4. Package body length/width does not include plastic flash protrusion across mold parting line.

PCB Metal Land Pattern (Dimensions in millimeters)



RECOMMENDED  
LAND PATTERN



RECOMMENDED  
LAND PATTERN MASK

All dimensions are in millimeters. Angles are in degrees.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1C	ANSI/ESD/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with both lead-free (260°C max. reflow temp.) and tin/lead (245°C max. reflow temp.) soldering processes. Solder profiles available upon request.

Contact plating: ENEPIG (NiPdAu)

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: [www.qorvo.com](http://www.qorvo.com)

Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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